

LIMITED SWITCH DYNAMIC LOGIC CIRCUIT WITH KEEPER**CROSS REFERENCE TO RELATED APPLICATION**

The present invention is related to the following: U.S. Patent Application
Serial No. 10655376 (Attorney Docket No. AUS920030498US1), filed
5 concurrently with this application, entitled "DUO-MODE KEEPER CIRCUIT," and

U.S. Patent Application Serial No. 10/116,612, filed April 4, 2002, entitled
"CIRCUITS AND SYSTEMS FOR LIMITED SWITCH DYNAMIC LOGIC,"
which are incorporated by reference herein.

TECHNICAL FIELD

10 The present invention relates in general to metal oxide silicon (MOS) dynamic
logic circuits.

BACKGROUND INFORMATION

Modern data processing systems may perform Boolean operations on a set of
signals using dynamic logic circuits. Dynamic logic circuits are clocked. During the
15 precharge phase of the clock, the circuit is preconditioned, typically by precharging
an internal node (dynamic node) of the circuit by coupling to a power supply rail.
During an evaluate phase of the clock, the Boolean function being implemented by
the logic circuit is evaluated in response to the set of input signal values appearing on
the inputs during the evaluate phase. (For the purposes herein, it suffices to assume
20 that the input signals have settled to their "steady-state" values for the current clock
cycle, recognizing that the input value may change from clock cycle to clock cycle.)
Such dynamic logic may have advantages in both speed and the area consumed on the
chip over static logic. However, the switching of the output node with the toggling of
the phase of the clock each cycle may consume power even when the logical value of
25 the output is otherwise unchanged.